This listing of claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS

1. (Previously Presented) A method for setting an operating parameter in a peripheral IC, the method comprising:

transmitting the operating parameter from a central IC using synchronous data transmission via a bus connection to the peripheral IC, the bus connection being a serial bus connection having a data line, a control line, and a clock line, wherein a data transmission clock signal is derived from a system clock signal available to the central IC;

buffering the operating parameter in a preregister of the peripheral IC, a current operating parameter being stored in a working register of the peripheral IC;

sending a start pulse signaling a start of a data transmission from the central IC to the peripheral IC via the control line; and

sending a transfer pulse from the central IC to the peripheral IC via the control line, the transfer pulse triggering transferring of the buffered operating parameter to the working register, wherein the buffered operating parameter becomes active in a working process of the peripheral IC;

wherein the start pulse is transmitted on the control line with a rising edge of the system clock signal during an active high state of the data transmission clock signal present on the clock line and wherein the transfer pulse is transmitted on the control line with a rising edge of the system clock signal when the data transmission clock signal is absent on the clock line.

2. (Cancelled).

3. (Cancelled).

4. (Previously Presented) The method according to claim 1, further comprising transferring a register write address for writing to the preregister in the peripheral IC on the data line ahead of the operating parameter.

5. (Cancelled).

6. (Previously Presented) A device for setting an operating parameter in a peripheral IC, the device comprising:

a serial bus connection between a central IC and the peripheral IC, the serial bus connection having a data line, a control line, and a clock line for synchronous data transmission, wherein a data transmission clock signal is derived from a system clock signal available in the central IC;

a preregister for buffering the operating parameter of the peripheral IC;

a working register for storing a current operating parameter of the peripheral IC;

means for transmitting a transfer pulse from the central IC to the peripheral IC over the control line, the transfer pulse triggering transferring of the buffered operating parameter to the working register, wherein the buffered operating parameter becomes active in a working process of the peripheral IC; and

signaling means for transmitting a start pulse for data transmission from the central IC to the peripheral IC over the control line;

wherein the start pulse is transmitted on the control line with a rising edge of the system clock during an active high state of the data transmission clock signal present on the clock line and wherein the transfer pulse is transmitted on the control line with a rising edge of a system clock signal when the data transmission clock signal is absent on the clock line.

7. (Cancelled).

8. (Cancelled).

9. (Previously Presented) The device according to claim 6, further including bus protocol means according to which a register write address for writing to the preregister is transferred to the peripheral IC on the data line ahead of the operating parameter.

10. (Cancelled).

11. (Previously Presented) The device according to claim 6, wherein the peripheral IC relates to a front-end IC for a communication arrangement for wireless data transmission and the central IC relates to a signal processing device, with means for one of modulation and demodulation of a mixed RF input signal and for further signal processing in baseband.

12. (Previously Presented) The device according to claim 11, wherein the operating parameter relates to a gain setting for a receive gain in the front-end IC.

13. (Previously Presented) The device according to claim 6, wherein the device is configured as a send and receive device for wireless data transmission in accordance with the HIPERLAN2 standard.